



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

25

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,247	04/11/2001	Michael R. Bruce	AMDA.486PA	3719
7590	01/18/2005		EXAMINER	
Crawford PLLC Suite 390 1270 Northland Drive St. Paul, MN 55120			HESSELTINE, RYAN J	
			ART UNIT	PAPER NUMBER
			2623	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/833,247	BRUCE ET AL.
	Examiner Ryan J Hesseltine	Art Unit 2623

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 14 September 2004.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 11 April 2001 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

**DETAILED ACTION**

***Response to Arguments***

1. Applicant's arguments on page 6, paragraph 3, filed September 14, 2004, with respect to the specification have been fully considered and are persuasive. The objection to the specification has been withdrawn.
2. Applicant's arguments on page 7, paragraph 4, filed September 14, 2004, with respect to claims 1, 14 and 15 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejection of claims 1, 14 and 15 in view of Phaneuf and Sandhu was in error and has been withdrawn.
3. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmermann et al. (USPN 6,162,735, newly cited, hereafter Zimmermann) in view of Phaneuf et al. (USPN 6,288,393, previously cited, hereafter Phaneuf).
6. Regarding claim 1, Zimmermann discloses a method for analyzing a suspected defect in an integrated circuit die (column 4, line 32-44), the method comprising: removing substrate from a selected portion of the die to expose the suspected defect (failure site); and recording a plurality

of images of the selected portion while substrate is being removed therefrom (column 5, line 15-46). Zimmermann does not disclose creating a three-dimensional image of the selected portion of the die with a plurality of images recorded by the imaging arrangement.

7. Phaneuf discloses an automated method of circuit analysis wherein a composite or mosaic image of a portion of a layer is generated from images of different locations on the same layer and portions of different layers are imaged and a three-dimensional image of the layers is created (column 9, line 34-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create a three-dimensional image of the selected portion of the die as taught by Phaneuf in order to determine a schematic or other representation (such as a failure site or defect) of the circuitry (column 5, line 42-48) or for reverse engineering and integrated circuit analysis (column 9, line 44-49).

8. Regarding claims 14 and 15, Zimmermann discloses a system for analyzing a suspected defect in an integrated circuit die (column 4, line 32-44), the system comprising: a substrate removal arrangement (means) adapted to remove substrate from a selected portion of the die to expose the suspected defect (failure site); an image recording arrangement (means) adapted to record a plurality of images of the selected portion while substrate is being removed therefrom (column 5, line 15-46); and an image creation arrangement (means) adapted to create a three-dimensional image of the selected portion of the die with a plurality of images recorded by the imaging arrangement (see above discussion of claim 1 with respect to Phaneuf).

9. Regarding claim 2, Zimmermann discloses that removing substrate includes cross-sectioning the die (column 4, line 45-51; column 5, line 15-21).

10. Regarding claims 3 and 16, Zimmermann discloses that the substrate removal arrangement includes using a FIB (focused ion beam) device (column 4, line 42-62; column 5, line 27-30).

11. Regarding claims 4 and 17, Zimmermann discloses that recording a plurality of images includes using a SEM (e-beam device) adapted to create a SEM image (column 4, line 42-62; column 5, line 40-46).

12. Regarding claims 5 and 18, Zimmermann discloses that the substrate removal arrangement and the image recording arrangement are included in a single dual FIB/e-beam device adapted to remove substrate with the FIB and to create a SEM image with the e-beam (column 4, line 42-column 5, line 14).

13. Regarding claims 6 and 19, Phaneuf discloses programming a controller adapted to control the dual FIB/e-beam device to affect the recording of a sufficient amount of SEM images (column 9, line 4-15) to create a three-dimensional image of the selected portion (column 9, line 34-49).

14. Regarding claim 7, Zimmermann discloses that removing substrate from the selected portion includes exposing a defect in the die (column 6, line 47-62), and wherein creating a three-dimensional image includes creating a three-dimensional image of the defect (see above discussion of claim 1).

15. Regarding claim 8, Phaneuf discloses that creating a three-dimensional image includes combining the plurality of images of the selected portion and creating a combined (composite or mosaic) image therefrom (column 9, line 34-49).

16. Regarding claim 9, Zimmermann discloses using the three-dimensional image (see above discussion of claim 1) to detect a defect in the die (column 6, line 58-62).

17. Regarding claim 10, Zimmermann discloses that creating a three-dimensional image (see above discussion of claim 1) includes creating an image of the defect (failure), further comprising using the image of the detected defect to analyze the defect (column 4, line 32-35; column 6, line 58-62; column 7, line 26-34).

18. Regarding claim 11, Phaneuf discloses that creating a three-dimensional image includes using selected ones of the plurality of images of the selected portion to create a three-dimensional image of less than (a portion of) the entire selected portion (column 9, line 34-49).

19. Regarding claim 12, neither Zimmermann nor Phaneuf disclose editing the three-dimensional image to create an edited image of only a portion of the three-dimensional image. The examiner takes Official Notice that editing techniques are well known in the art of image processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made to edit the three-dimensional image to create an edited image of only a portion of the three-dimensional image in order to display only a relevant portion of the three-dimensional image such as the portion exhibiting a defect or the like.

20. Regarding claim 13, Zimmermann discloses that editing the three-dimensional image (see above discussion of claim 12) includes creating an image of a cross-section of the selected portion (column 4, line 45-51; column 5, line 15-21).

21. Regarding claim 20, Phaneuf discloses that the image creation arrangement includes a computer adapted to create the three-dimensional image in response to image characteristic selections (column 9, line 34-49).

***Conclusion***

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

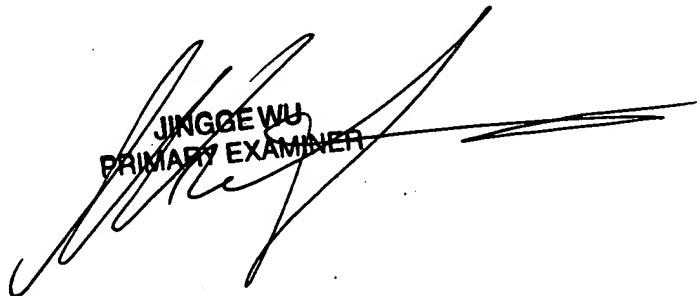
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J Hesseltine whose telephone number is 703-306-4069. The examiner can normally be reached on Monday - Friday, 8:30 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on 703-308-6604. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan J. Hesseltine  
January 13, 2005



JINGGE WU  
PRIMARY EXAMINER